B3 cont

(a) forming a first gate insulating film for forming the MIS transistor structure on a main surface of a semiconductor substrate;

(b) forming at least one pair of laminating structure bodies each including two layers of a first gate electrode covering a part of said first gate insulating film and a first insulating film covering said first gate electrode, an etching prevention film being formed on a sidewall portion of said first insulating film but so as not to cover sidewall portions of said first gate electrode;

(c) introducing impurities into said semiconductor substrate through said first gate insulating film located in a region not covered with said laminating structure bodies, and thereby forming a first impurity introduced region self-aligned with said laminating structure bodies on the main surface of said semiconductor substrate;

(d) removing said first gate insulating film in the region not covered with said laminating structure bodies after said step (c); and

(e) forming a second insulating film covering upper portions and sidewall portions of said laminating structure bodies after said step (d).

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B9 cont

9. ~~19~~. (Amended) A method for manufacturing a semiconductor integrated circuit device, comprising the steps of:

(a) forming, on a main surface of a semiconductor substrate, a first gate insulating film consisting of a silicon oxide film, and forming a first conductive film, a second gate insulating film and a second conductive film over said first gate insulating film in this order:

(b) forming a first protection insulating film consisting of a single layer silicon oxide film formed over said second conductive film, with or without a laminating silicon nitride film formed over the silicon oxide film;

(c) patterning said first protection insulating film, and thereby forming an etching mask consisting of said first protection insulating film;

(d) patterning said second conductive film, said second gate insulating film and said first conductive film in this order by dry etching using said etching mask as a mask, and thereby forming a plurality of gate electrodes that each have a floating gate electrode formed by a portion of said first conductive film and a control gate electrode formed by a portion of said second conductive film and that each have a laminating structure in which an

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upper portion of said control gate electrode is covered with said first protection insulating film;

(e) forming an etching prevention film consisting of a silicon nitride film on the patterned first protection insulating film, after said step (c) and before said step (d), or after said step (d), said etching prevention film being formed on both sidewall portions of the patterned first protection insulating film but so as not to cover sidewall portions of said floating gate electrode and said control gate electrode formed in said step (d);

(f) introducing impurities into the main surface of said semiconductor substrate located between sidewall portions facing each other in said plurality of gate electrodes, and thereby forming a source region and a drain region;

(g) treating a surface of said semiconductor substrate by using etchant containing a hydrofluoric acid after said step (f), and thereby cleaning said first gate insulating film located between the sidewall portions which face each other in said plurality of gate electrodes;

(h) covering an upper portion and both sidewall portions of each of said plurality of gate electrodes after said step (g), and forming a second protection insulating

film consisting of a silicon nitride film having such a thickness as to partially embed a region between the sidewall portions which face each other in said plurality of gate electrodes;

(i) forming, on an upper portion of said second protection insulating film, an interlayer insulating film consisting of a silicon oxide film, and embedding, with said interlayer insulating film, the region between the sidewall portions which face each other in said plurality of gate electrodes;

(j) etching said interlayer insulating film and said second protection insulating film located between the sidewall portions which face each other in said plurality of gate electrodes, and thereby forming a first connection hole for exposing a surface of said source region and a second connection hole for exposing a surface of said drain region; and

(k) forming a third conductive film electrically connected to said source region inside said first connection hole, and forming a fourth conductive film electrically connected to said drain region inside said second connection hole.

B5 cont.

11. ~~21.~~ (Amended) The method for manufacturing a semiconductor integrated circuit device according to claim 10 ~~20~~,

wherein each of said plurality of gate electrodes constitutes part of a respective memory cell of a flash memory, and writing into said memory cell is carried out by injecting a charge into said floating gate electrode thereof, and erasing from said memory cell is carried out by discharging, to said semiconductor substrate, said charge injected into said floating gate electrode thereof.

Please add the following new claims:

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15. ~~25.~~ (New) The method for manufacturing a semiconductor integrated circuit device according to claim 9 ~~19~~,

wherein said step (g) is conducted so that said first gate insulating film retreats beneath opposite sidewall portions of said floating gate electrode.

16. ~~26.~~ (New) A method for manufacturing a semiconductor integrated circuit device having an MIS transistor structure of a flash memory, comprising the steps of:

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(a) forming, on a main surface of a semiconductor substrate, a first gate insulating film, and forming a first conductive film, a second gate insulating film and a second conductive film over said first gate insulating film in this order;

(b) forming a first protection insulating film consisting of a single layer silicon oxide film formed over said second conductive film, with or without a laminating silicon nitride film formed over the silicon oxide film;

(c) patterning said first protection insulating film, and thereby forming an etching mask consisting of said first protection insulating film;

(d) patterning said second conductive film, said second gate insulating film and said first conductive film in this order by dry etching using said etching mask as a mask, and thereby forming a plurality of gate electrodes that each have a floating gate electrode formed by a portion of said first conductive film and a control gate electrode formed by a portion of said second conductive film and that each have a laminating structure in which an upper portion of said control gate electrode is covered with said first protection insulating film;

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(e) forming an etching prevention film consisting of a silicon nitride film on the patterned first protection insulating film, after said step (c) and before said step (d), or after said step (d), said etching prevention film being formed on both sidewall portions of the patterned first protection insulating film but so as not to cover sidewall portions of said floating gate electrode and said control gate electrode formed in said step (d);

(f) introducing impurities into the main surface of said semiconductor substrate located between sidewall portions facing each other in said plurality of gate electrodes, and thereby forming a source region and a drain region;

(g) treating a surface of said semiconductor substrate by using etchant after said step (f);

(h) covering an upper portion and both sidewall portions of each of said plurality of gate electrodes after said step (g), and forming a second protection insulating film consisting of a silicon nitride film having such a thickness as to partially embed a region between the sidewall portions which face each other in said plurality of gate electrodes;

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(i) forming, on an upper portion of said second protection insulating film, an interlayer insulating film consisting of a silicon oxide film, and embedding, with said interlayer insulating film, the region between the sidewall portions which face each other in said plurality of gate electrodes;

(j) etching said interlayer insulating film and said second protection insulating film located between the sidewall portions which face each other in said plurality of gate electrodes, and thereby forming a first connection hole for exposing a surface of said source region and a second connection hole for exposing a surface of said drain region.

17.
~~27.~~ (New) The method for manufacturing a semiconductor integrated circuit device according to claim 16
~~26~~, further comprising the steps of:

(k) forming a third conductive film electrically connected to said source region inside said first connection hole, and forming a fourth conductive film electrically connected to said drain region inside said second connection hole.

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18.
~~28.~~ (New) The method for manufacturing a semiconductor integrated circuit device according to claim 17, ~~27,~~

wherein said third conductive film formed inside said first connection hole functions as a part of a source line, and said fourth conductive film formed inside said second connection hole functions as a part of a data line.

19.
~~29.~~ (New) The method for manufacturing a semiconductor integrated circuit device according to claim 18 ~~28,~~

wherein each of said plurality of gate electrodes constitutes part of a respective memory cell of a flash memory, and writing into said memory cell is carried out by injecting a charge into said floating gate electrode thereof, and erasing from said memory cell is carried out by discharging, to said semiconductor substrate, said charge injected into said floating gate electrode thereof.

20.
~~30.~~ (New) The method for manufacturing a semiconductor integrated circuit device according to claim 16 ~~26,~~

wherein said flash memory is a NOR type flash memory.

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21.
~~31.~~ (New) The method for manufacturing a semiconductor integrated circuit device according to claim 16 ~~26~~,

wherein said step (g) is conducted so that said first gate insulating film retreats beneath opposite sidewall portions of said floating gate electrode.

22.
~~32.~~ (New) The method for manufacturing a semiconductor integrated circuit device according to claim 1 ~~11~~,

wherein said step (d) is conducted such that said first gate insulating film retreats beneath opposite sidewall portions of said first gate electrode.

B